

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Gilbert Wolrich et al.  
Serial No.: 10/057,738  
Filed : January 25, 2002  
Assignee : Intel Corporation  
Title : DATA TRANSFER MECHANISM

Art Unit: 2187  
Examiner: Ngoc V. Dinh

Mail Stop RCE  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Dear Sir:

Applicants call attention to the attached Information  
Disclosure Statement and documents listed on form PTO-1449.

This filing is being made with a Request for Continued  
Examination. No fee is required.

Also enclosed is a copy of the Electronic Information  
Disclosure Statement filed June 3, 2004 (8 pages). Applicants  
respectfully request consideration of the prior art listed  
therein.

CERTIFICATE OF MAILING BY FIRST CLASS MAIL

I hereby certify under 37 CFR §1.8(a) that this correspondence is being  
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Applicant : Gilbert Wolrich et al.  
Serial No. : 10/057,738  
Filed : January 25, 2002  
Page : 2 of 2

Attorney Docket: 10559-618001 / P12857

The documents are in the English language; hence no concise explanation is necessary per Rule 98(a)(3).

Consideration of the foregoing and enclosures plus the return of a copy of the enclosed form PTO-1449 with the Examiner's initials in the left column per MPEP 609 are earnestly solicited along with an early action on the merits.

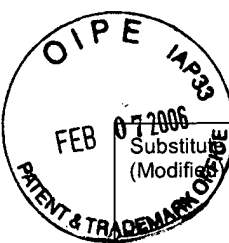
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Respectfully submitted,

Date: 2/3/2006

Rex I. Huang  
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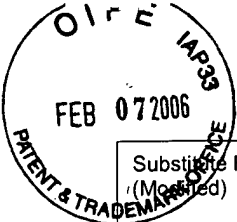
Fish & Richardson P.C.  
225 Franklin Street  
Boston, MA 02110  
Telephone: (617) 542-5070  
Facsimile: (617) 542-8906



<b>Information Disclosure Statement by Applicant</b> (Use several sheets if necessary)  (37 CFR §1.98(b))	Substitute Form PTO-1449	U.S. Department of Commerce Patent and Trademark Office	Attorney's Docket No. 10559-618001	Application No. 10/057,738
	Applicant Gilbert Wolrich et al.			
	Filing Date January 25, 2002		Group Art Unit 2187	

U.S. Patent Documents							
Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
	AA	2001/0043614	11/2001	Viswanadham et al.			
	AB	2003/0012198	01/2003	Kaganoi et al.			
	AC	2003/0041216	02/2003	Rosenbluth et al.			
	AD	2003/0065862	04/2003	Wyland			
	AE	2003/0078950	04/2003	Abernathy et al.			
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	AL	5,008,808	04/1991	Fries et al.			
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	AT	5,813,031	09/1998	Chou et al.			
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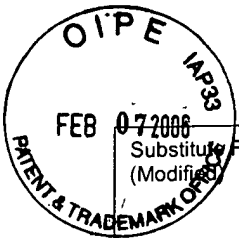
Examiner Signature	Date Considered
EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	



<b>Information Disclosure Statement by Applicant</b> (Use several sheets if necessary)  (37 CFR §1.98(b))	Substitute Form PTO-1449 (Modified)	U.S. Department of Commerce Patent and Trademark Office	Attorney's Docket No. <b>10559-618001</b>	Application No. <b>10/057,738</b>
	Applicant <b>Gilbert Wolrich et al.</b>			
	Filing Date <b>January 25, 2002</b>		Group Art Unit <b>2187</b>	

U.S. Patent Documents							
Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
	ABB	6,173,349	01/2001	Qureshi et al.			
	ACC	6,212,602	04/2001	Wicki et al.			
	ADD	6,247,086	06/2001	Allingham			
	AEE	6,249,829	06/2001	Bloks et al.			
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	AHH	6,356,962	03/2002	Kasper et al.			
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U.S. Patent Documents							
Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
	ACCC	6,754,662	06/2004	Li, Fulu			
	ADDD	6,754,795	06/2004	Chen et al.			
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	AGGG	6,823,399	11/2004	Horiguchi et al.			
	AHHH	6,826,180	11/2004	Bergantino et al.			
	AIII	6,847,645	01/2005	Potter et al.			
	AJJJ	6,958,973	10/2005	Chen et al.			

Other Documents (include Author, Title, Date, and Place of Publication)		
Examiner Initial	Desig. ID	Document
	AKKK	<i>C-5 Network Processor Architecture Guide</i> , C-Port Corporation, Freescale Semiconductor, Inc., Part No. C5NPD0-AG/D, May 31, 2001, 642 pages.
	ALLL	Chang, Shu-Ping et al., "An Overview of the Pipelined Common Buffer Architecture (PCBA) for Memory Based Packet/Cell Switching Systems", <i>IEEE</i> , pp. 288-297 (1994).
	AMMM	Frazier, Gregory L. et al., "The Design and Implementation of a Multi-Queue Buffer For VLSI Communication Switches", <i>IEEE</i> , pp. 466-471 (1989).
	ANNN	Lin, Yu-Sheng et al., "Queue Management for Shared Buffer and Shared Multi-buffer ATM Switches", <i>IEEE</i> , pp. 688-695 (1996).

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